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Zero-Voltage Switching Full-Bridge T-type DC/DC Converter with Wide Input Voltage Range and Balanced Switch Currents

Dong Liu, *Member, IEEE*, Yanbo Wang, *Member, IEEE*, Fujin Deng, *Member, IEEE*, Qi Zhang, *Member, IEEE*, and Zhe Chen, *Senior Member, IEEE*

***Abstract*— With the development of silicon carbide (SiC) power devices, the circuit structure of power converter for high voltage applications would be simpler and more compact because the two-level based topologies become applicable. This paper proposes a full-bridge (FB) T-type isolated DC/DC converter for the applications with high input voltage and wide input voltage range. The proposed converter is composed of four main power switches with high voltage stress (SiC MOSFET) and four auxiliary power switches with low voltage stress (Si MOSFET). Comparing with the conventional diode clamped FB three-level (TL) isolated DC/DC converters, the proposed FB T-type converter has simpler circuit structure and higher efficiency. A corresponding control strategy including two working patterns is proposed, which can not only realize the zero-voltage switching (ZVS) for the main and auxiliary power switches but also satisfy the wide input voltage range. More importantly, the proposed corresponding control strategy has the ability of balancing the currents among the power switches, which would balance the power losses, thermal stresses among the power switches and thus improve the reliability of converter. The characteristics and performances of proposed converter with the corresponding control strategy are analyzed in detail and verified by the simulation and experimental results.**

***Index Terms*— Full-bridge DC/DC converter; Switch current balance; T-type; Wide input voltage range; Zero-voltage switching (ZVS).**

I. Introduction

The research about the high power isolated DC/DC converter with the high efficiency and high reliability is one of the hot topics in the modern power electronics because the isolated DC/DC converters are widely applied in the electric vehicles, telecom, solar system, fuel cell system, DC transmission system, and others due to their merits of the galvanic isolation and flexible voltage conversion rate [1-6].

The most popular and useful isolated DC/DC converter is two-level zero-voltage switching (ZVS) DC/DC converter with the phase-shift control [7-11] due to the simple circuit structure, high power density, and easy control strategy. However, the power switches in the two-level converters need to withstand the full input voltage, which makes them not suitable for the applications with the high input voltage. In order to solve this drawback of the two-level DC/DC converter, the three-level (TL) ZVS DC/DC converter was proposed for the high input voltage applications because the voltage stresses on the power switches are only half of the input voltage in the TL DC/DC converter [12-14]. Therefore, the power switches with the low-voltage stress and small on-state resistance can be applicable in the TL DC/DC converter. Many studies have been carried on the TL isolated DC/DC converters in the topics of extending the soft switching range [15], [16], reducing the circulating currents [17], [18], balancing the voltages on the input capacitors [19], [20], minimizing and balancing the currents flowing through the input capacitors [21], [22]. In [23], a hybrid FB isolated TL DC/DC converter was proposed for the applications with high voltage and wide input voltage range. Two control strategies in [24], [25] were proposed for the conventional diode clamped FB TL isolated DC/DC converter. However, the currents among the primary power devices in [23-25] are unbalanced, which would cause the power loss imbalance and thermal stress imbalance among the power switches and thus affect the reliability of the converter.

There is another kind of the TL converter named T-type converter, which has been widely used in the single-phase or three-phase inverters [26-28]. The T-type isolated DC/DC converters were proposed in [29] and [30], which are more suitable for the industrial applications due to their simpler circuit structure and higher power density in comparison with the conventional TL isolated DC/DC converter. However, the T-type DC/DC converters in [29] and [30] are both half-bridge (HB) structure which is not suitable for the high power applications because the current stress on the power switches in the half-bridge structure is twice of that in the full-bridge structure. Additionally, the T-type converter is derived from

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Dong Liu, Yanbo Wang, and Zhe Chen are with the Department of Energy Technology, Aalborg University, Aalborg, 9220 Denmark (email: dli@et.aau.dk, ywa@et.aau.dk, zch@et.aau.dk).

Fujin Deng is with the School of Electrical Engineering, Southeast University, Nanjing, 210000 China (email: dfjqfa@163.com).

Qi Zhang is with the Department of Electrical Engineering, Xi'an University of Technology, Xi'an, 710000 China (email: zhangqi@xaut.edu.cn).

the two-level based topology, so it has the disadvantage of the two-level converter that the main power switches in the T-type DC/DC converter also need to withstand the full input voltage. Fortunately, with the advent and development of the silicon carbide (SiC) power devices, the T-type isolated DC/DC converter with SiC power devices would become applicable for the applications with high input voltage since the drain-source breakdown voltage of the SiC power devices are much higher than that of the silicon (Si) power devices [31]. Nowadays, the dominant and maximum drain-source voltage of commercially available SiC Mosfet is 1200 V and 1700 V, respectively [31]. Therefore, the T-type DC/DC converter with SiC Mosfet can be utilized into the industrial applications with the input voltage below 1200 V after considering the derating for selecting power switch. When the input voltage increases to several kilo volts, the TL based DC/DC converters would become the better choice because its advantage of lower voltage stress on the power switches makes it possible to select suitable power switches. However, the commercial SiC Mosfet with higher drain-source voltage is being developed, so the applicable range of the T-type DC/DC converter with SiC Mosfet would become larger with the increasing of SiC Mosfet's drain-source voltage.

In this paper, a full-bridge (FB) T-type isolated DC/DC converter is proposed for the high power applications with the high input voltage and wide input voltage range. The proposed converter is composed of four main power switches with high voltage stress (SiC MOSFET) and four auxiliary power switches with low voltage stress (Si MOSFET), which thus has more compact circuit structure and higher efficiency in comparison with the conventional diode clamped FB TL isolated DC/DC converters. A corresponding control strategy including two working patterns is proposed. The proposed control strategy can not only achieve the zero-voltage switching (ZVS) for the main and auxiliary power switches but also satisfy the wider input voltage range in comparison with the FB two-level isolated DC/DC converter. In addition, the proposed corresponding control strategy has the ability of keeping the currents among the power switches balanced, which would thus balance the power losses and thermal stresses among the power switches. The characteristics and performances of the proposed converter with the corresponding control strategy are analyzed in detail. Finally, the simulation and experimental results are presented to verify the proposed converter and corresponding control strategy. Table I shows the general comparison about the existing HB T-type isolated DC/DC converter, conventional diode-clamped FB TL isolated DC/DC converters, and proposed FB T-type isolated DC/DC converter.

This paper is organized as follows. Section II analyzes the operation principle of the proposed FB T-type isolated DC/DC converter with the corresponding control strategy. Section III introduces the switch current balancing ability in detail. Section IV analyzes the characteristics and performances of the proposed converter with the corresponding control strategy. Section V presents the simulation and experimental results to verify the proposed converter with the corresponding control strategy. Finally, the main contributions of this paper are summarized in Section VI.

II. Operation Principle

Fig. 1(b) shows the circuit structure of the proposed FB T-type isolated DC/DC converter. In the primary side, C_1 and C_2 are two input capacitors which split the input voltage V_{in} into V_1 and V_2; S_1 - S_4 are four main power switches, S_5 - S_8 are four auxiliary power switches, and D_1 - D_8 are eight power diodes; C_{s1} - C_{s8} are the parasitic capacitors of S_1 - S_8; T_r is the transformer; L_r is the leakage inductance of the transformer T_r. In the secondary side, D_{r1} - D_{r4} are four output rectifier diodes; L_o and C_o are the output filter inductor and capacitor, respectively. In Fig. 1(b), V_{in} is the input voltage; V_{ab} is the voltage between point a and b; i_p is the primary current of the transformer T_r; V_o' is the secondary voltage after rectification; i_{S1} - i_{S8} are the currents flowing through (S_1, D_1) - (S_8, D_8); i_{Lo} is the current flowing through the output filter inductor L_o; V_o and I_o are the output voltage and current; n is the turns ratio of the transformer T_r.

TABLE I
GENERAL COMPARISON ABOUT THE EXISTING CONVERTERS AND PROPOSED CONVERTER

Primary Side	HB T-type isolated DC/DC converter [29], [30]	Diode clamped FB TL isolated DC/DC converter [24], [25] as shown in Fig. 1(a)	Hybrid TL FB isolated DC/DC converter [23]	Proposed FB T-type isolated DC/DC converter
Primary circuit type	**Half bridge**	**Full bridge**	**Full bridge**	**Full bridge**
Power switch number	**4**	**8**	**6**	**8**
Clamping diode number	**0**	**4**	**2**	**0**
Flying capacitor number	**0**	**2**	**1**	**0**
Input capacitor number	**2**	**2**	**2**	**2**
Total main primary component number	**6**	**16**	**11**	**10**
Suitable power level	**Low**	**High**	**High**	**High**
Switch current balancing ability	**Yes**	**No**	**No**	**Yes**
Wide input voltage range	**No**	**Yes**	**Yes**	**Yes**

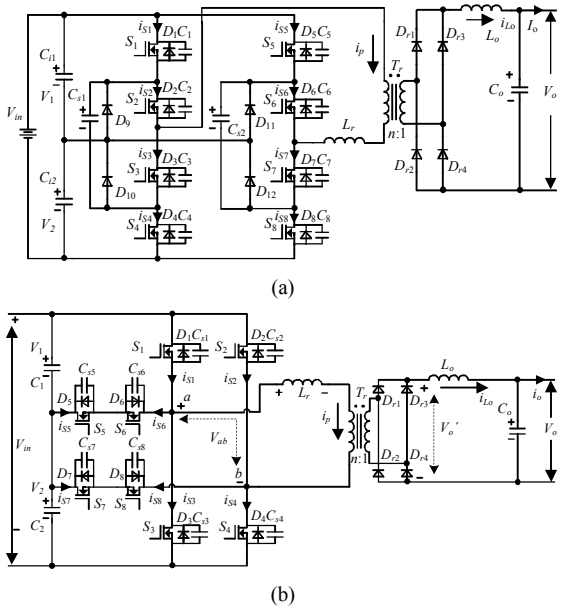


Fig. 1. Circuit structure. (a) Conventional diode clamped FB TL isolated DC/DC converter. (b) Proposed FB T-type isolated DC/DC converter.

In order to simplify the following analysis, some assumptions are made: 1) all the capacitors and inductors are ideal; 2) all the power diodes are ideal; 3) the main power switches S_1 - S_4 and auxiliary power switches S_5 - S_8 have the same parasitic capacitors respectively, which means $C_{s1} = C_{s2} = C_{s3} = C_{s4} = C_{j1}$ and $C_{s5} = C_{s6} = C_{s7} = C_{s8} = C_{j2}$; 4) the two input capacitors C_1 and C_2 are large enough to be considered as two voltage sources with the value of $V_{in}/2$; and 5) the output filter inductor L_o is large enough to be considered as a constant current source.

The proposed corresponding control strategy is composed of two working patterns as shown in Figs. 2(a) and (b). In Fig. 2, d_{rv1} - d_{rv8} are driving signals of the power switches S_1 - S_8; d_1, d_2 are duty cylces in one switching period T_s under the working pattern I and II respectively; d_{loss_I} and d_{loss_II} are duty cycle losses in one switching period T_s under the working pattern I and II respectively.

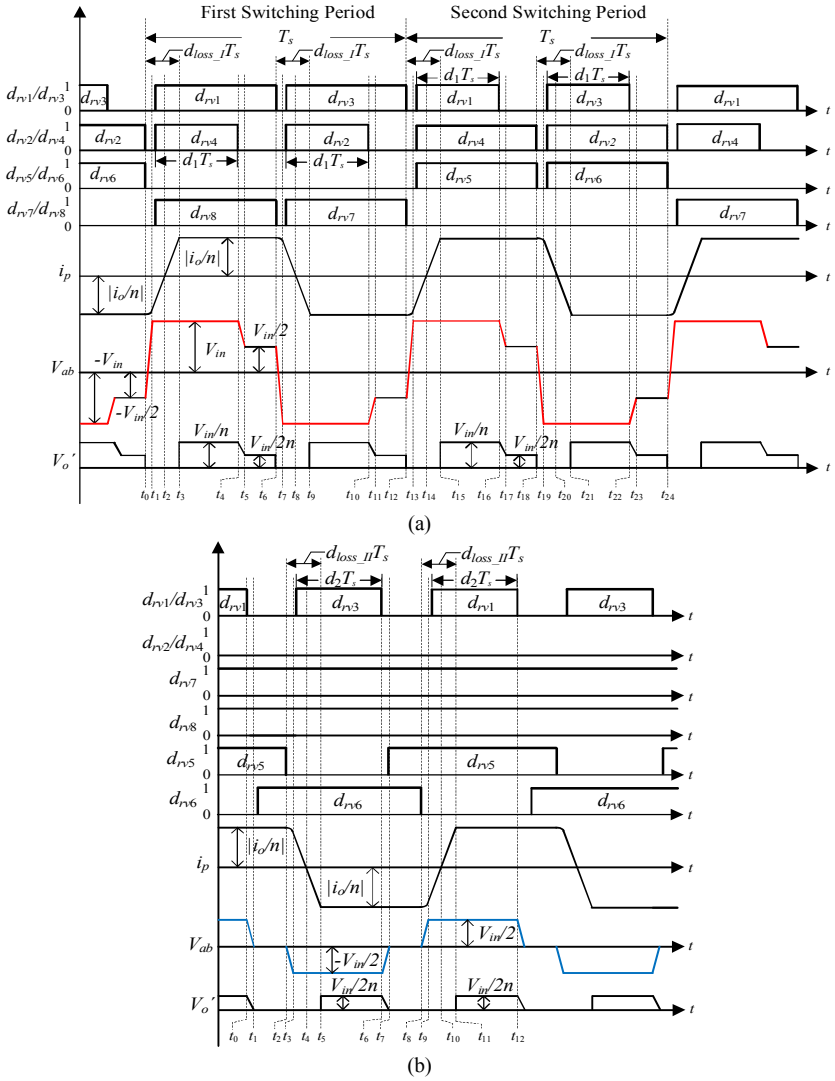


Fig. 2. Main waveforms of proposed T-type converter under corresponding control strategy. (a) Working pattern I. (b) Working pattern II.

1) *Working pattern I* is used for the low input voltage. In the first switching period of working pattern I, the duty cycles for the driving signals of the power switches S_1, S_3, S_7, and S_8 are both 0.5 if neglecting the dead time; the duty cycles for the driving signals of the power switches S_2, S_4 are both d_1. In the second switching period of working pattern I, the duty cycles for the driving signals of the power switches S_2, S_4, S_5, and S_6 are both 0.5 if neglecting the dead time; the duty cycles for the driving signals of the power switches S_1, S_3 are both d_1. The driving signals for the power switches are the same in every two swtiching periods. By adjusting the duty cycle d_1, the time length of the third-level voltage (V_{in} and $-V_{in}$) as marked in Fig. 2(a) would be changed, which can thus adjust the output voltage V_o. For instance, if reducing d_1, the time length of the third-level voltage (V_{in} and $-V_{in}$) would decrease, which means the output voltage V_o would decrease. One thing needing to be mentioned is that the output characteristic are the same under the first and second switching period because the primary voltage on the transformer (V_{ab}) under the first and second switching period are the same as shown in Fig. 2(a).
2) *Working pattern II* is used for the high input voltage when the duty cycle d_1 reduces to 0. In the working pattern II, the duty cycles for the driving signals of the power switches S_2 and S_4 are both 0; the duty cycles for the driving signals of the power switches S_7 and S_8 are both 1; the duty cycles for the driving signals of the power switches S_1 and S_3 are both d_2; and (S_3, S_5), and (S_1, S_6) are complementary switch pairs. By adjusting the duty cycle d_2, the time length of the second-level voltage ($V_{in}/2$ and $-V_{in}/2$) as marked in Fig. 2(b) would be changed, which can thus adjust the output voltage V_o. For instance, if reducing d_2, the time length of the second-level voltage ($V_{in}/2$ and $-V_{in}/2$) would decrease, which means the output voltage V_o would decrease. Comparing with the FB two-level DC/DC converter, the proposed converter can satisfy the wider input voltage range because the primary voltage on transformer V_{ab} is only half of the input voltage ($V_{in}/2$) in the working pattern II, which would be analyzed in detail in Section IV-C.

A. *Working Pattern I*

Fig. 3 shows the equivalent operation circuits in the working pattern I shown in Fig. 2(a).

Stage 0 [before t_0]: During this period, both S_2 and S_6 are on-state, so the primary voltage V_{ab} equals to minus half of the input voltage $-V_{in}/2$. The primary current i_p is $-i_o/n$ and the input power transfers to the load from T_r, D_{r2}, and D_{r3}.

Stage 1 [t_0 - t_1]: At t_0, the power switches S_2 and S_6 are turned off. Then C_{s2}, C_{s3}, C_{s6}, C_{s7} are charged and C_{s1}, C_{s4}, C_{s8} are discharged. The primary current i_p starts to increase and is not enough to provide output current i_o, so the output rectifier diodes D_{r1}, D_{r2}, D_{r3}, and D_{r4} conduct simultaneously, which clamps both the primary and secondary voltage of the transformer at 0 V.

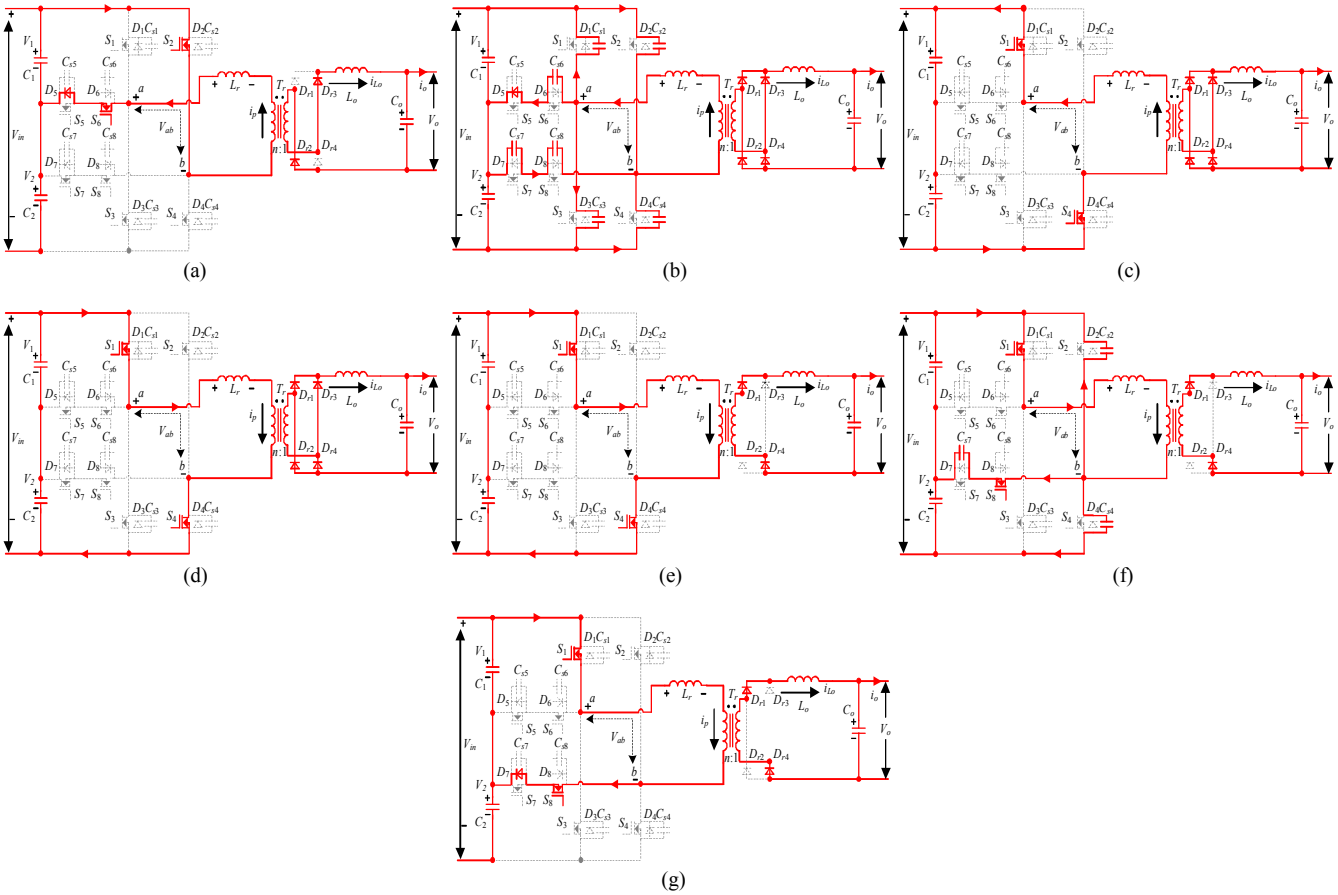


Fig. 3. Equivalent operation circuits of working pattern I. (a) [before t_0] (b) [t_0-t_1]. (c) [t_1-t_2]. (d) [t_2-t_3]. (e) [t_3-t_4]. (f) [t_4-t_5]. (g) [t_5-t_6].

Stage 2 [t_1 - t_2]: At t_1, the voltages on C_{s2} (V_{cs2}) and C_{s3} (V_{cs3}) increase to the input voltage V_{in}, the voltages on C_{s6} (V_{cs6}) and C_{s7} (V_{cs7}) increase to half of the input voltage V_{in}/2, the voltages on C_{s1} (V_{cs1}), C_{s4} (V_{cs4}), and C_{s8} (V_{cs8}) decrease to 0 V. Then D_1 and D_4 conduct, which clamps the voltage of S_1 and S_4 at 0 V. Therefore, the power switches S_1 and S_4 can be turned on with the zero-voltage. During this stage, the primary voltage V_{ab} is V_{in}, which is fully applied on the L_r, so the primary current i_p increases linearly.

Stage 3 [t_2 - t_3]: At t_2, the primary current i_p increases to 0 A, which means the current direction of i_p would change. During this stage, the primary voltage V_{ab} remains V_{in} and the primary current i_p still increases linearly.

Stage 4 [t_3 - t_4]: At t_3, the primary current i_p increases to the positive reflected output current whose value is i_o/n. Then D_{r2} and D_{r3} are turned off, and the input power starts to transfer to load from T_r, D_{r1} and D_{r4}.

Stage 5 [t_4 - t_5]: At t_4, the power switch S_4 is turned off. Then i_o is reflected to the primary side, which means that i_p is still i_o/n to charge C_{s4} and discharge C_{s2}, C_{s7}. Therefore, the voltage on C_{s4} (V_{cs4}) increases, the voltage on C_{s2} (V_{cs2}) and C_{s7} (V_{cs7}) decrease.

Stage 6 [t_5 - t_6]: At t_5, V_{cs4} increases to V_{in}/2, V_{cs2} and V_{cs7} decrease to V_{in}/2 and 0 V respectively. Then D_7 conducts, which clamps the voltage of S_7 at 0 V. During this stage, the primary voltage V_{ab} is half of the input voltage V_{in}/2, the primary current i_p remains i_o/n.

At t_6, the power switches S_1 and S_8 are turned off, then the second half cycle [t_6 - t_{12}] starts. The following analysis is similar to the first half cycle [t_0 - t_6], which is not repeated here. In addition, the second switching period [t_{12} - t_{24}] is similar to that of the first switching period [t_0 t_{12}], which is not repeated here.

B. *Working Pattern II*

Fig. 4 shows the equivalent operation circuits in the working pattern II shown in Fig. 2(b).

Stage 0 [before t_0]: During this period, S_1, S_5, S_7, and S_8 are all on-state, so the primary voltage V_{ab} equals to half of the input voltage V_{in}/2. The primary current i_p is i_o/n and the input power transfers to the load from T_r, D_{r1}, and D_{r4}.

Stage 1 [t_0 - t_1]: At t_0, the power switch S_1 is turned off. Then i_o is reflected to the primary side, which means that i_p is still i_o/n to charge C_{s1} and discharge C_{s3}, C_{s6}. Therefore, the voltage on C_{s1} (V_{cs1}) increases, the voltages on C_{s3} (V_{cs3}) and C_{s6} (V_{cs6}) decrease.

Stage 2 [t_1 - t_2]: At t_1, V_{cs1} increases to V_{in}/2, V_{cs3} and V_{cs6} decrease to V_{in}/2 and 0 V respectively. Then D_6 conducts, which clamps the voltage of S_6 at 0 V. Therefore the power switch S_6 can be turned on with the zero-voltage. During this stage, the primary voltage V_{ab} is 0 V, the primary current i_p remains i_o/n.

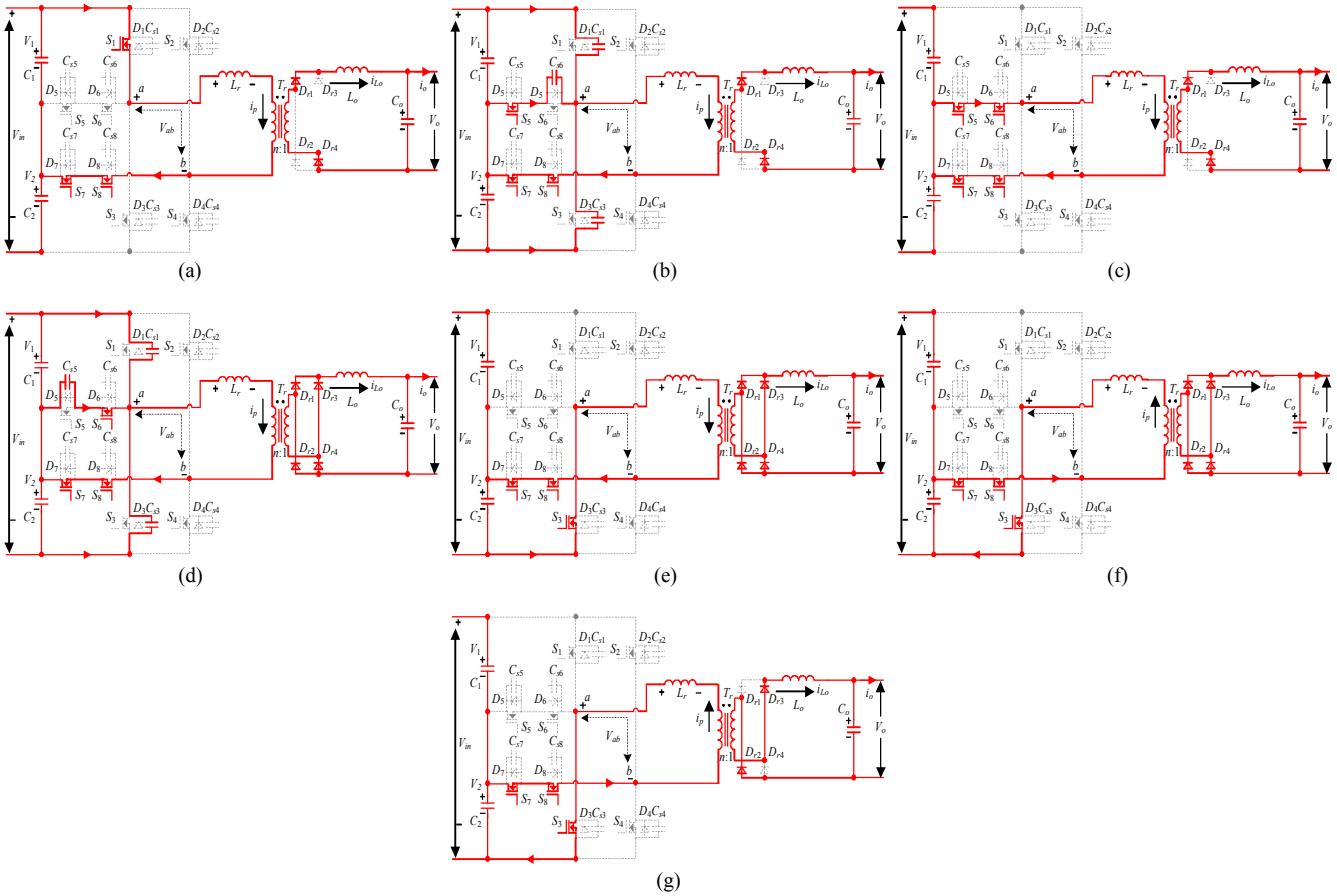


Fig. 4. Equivalent operation circuits of working pattern II. (a) [before t_0] (b) [t_0-t_1]. (c) [t_1-t_2]. (d) [t_2-t_3]. (e) [t_3-t_4]. (f) [t_4-t_5]. (g) [t_5-t_6].

Stage 3 [t_2 - t_3]: At t_2, the power switch S_5 is turned off. Then C_{s1}, C_{s5} are charged and C_{s3} is discharged. The primary current i_p starts to decrease and is not enough to provide output current i_o, so the output rectifier diodes D_{r1}, D_{r2}, D_{r3}, and D_{r4} conduct simultaneously, which clamps both the primary and secondary voltage of the transformer at 0 V.

Stage 4 [t_3 - t_4]: At t_3, the voltages on C_{s1} (V_{cs1}) and C_{s5} (V_{cs5}) increase to V_{in} and $V_{in}/2$ respectively, the voltage on C_{s3} (V_{cs3}) decreases to 0 V. Then D_3 conducts, which clamps the voltage of S_3 at 0 V. Therefore, the power switch S_3 can be turned on with the zero-voltage. During this stage, the primary voltage V_{ab} is $-V_{in}/2$, which is fully applied on the L_r, so the primary current i_p decreases linearly.

Stage 5 [t_4 - t_5]: At t_4, the primary current i_p deceases to 0 A, which means the current direction of i_p would change. During this stage, the primary voltage V_{ab} remains $-V_{in}/2$ and the primary current i_p still decreases linearly.

Stage 6 [t_5 - t_6]: At t_5, the primary current i_p decreases to the negative reflected output current whose value is $-i_o/n$. Then D_{r1} and D_{r4} are turned off, and the input power starts to transfer to load from T_r, D_{r2} and D_{r3}.

At t_6, the power switch S_3 is turned off, then the second half cycle [t_6 - t_{12}] starts. The following analysis is similar to the first half cycle [t_0 - t_6], which is not repeated here.

III. Switch Current Balancing Ability

The proposed corresponding control strategy has the switch current balancing ability in the working pattern I, which can keep the currents among the power switches balanced. Fig. 5 shows the currents flowing through the power switches in the working pattern I. From Fig. 5, it can be seen that there are two operation modes (named operation mode I and II) in the working pattern I. By swapping these two operation modes in every switching period, the currents among the main power switches and auxiliary power switches can be kept balanced respectively in every two switching periods as marked in Fig. 5, which means that: 1) in the operation mode I, the duty cycles of d_{rv1}, d_{rv3}, d_{rv7}, and d_{rv8} are both 0.5 if neglecting the dead time, the duty cycles of d_{rv2} and d_{rv4} are both d_1; and 2) in the operation mode II, the duty cycles of d_{rv2}, d_{rv4}, d_{rv5}, and d_{rv6} are both 0.5 if neglecting the dead time, the duty cycles of d_{rv1} and d_{rv3} are both d_1.

Before calculating the RMS currents on the power switches, the duty cycle loss needs to be analyzed. Under the working pattern I, [t_0 - t_3], [t_6 - t_9] and [t_{12} - t_{15}], [t_{18} - t_{21}] are the time periods of the duty cycle loss in operation mode I and II respectively, in which the primary current of the transformer i_p changes from the positive (or negative) direction to the negative (or positive) reflected output filter inductor current. During the time periods of the duty cycle loss, all the four output rectifier diodes D_{r1} - D_{r4} conduct, so the primary and secondary voltage of the transformer are both clamped at 0 V and there is no power transferring from the input power to the load during these time periods. If neglecting the quite short time periods [t_0 - t_1], [t_6 - t_7], [t_{12} - t_{13}], and [t_{18} - t_{19}], the time periods [t_0 - t_3], [t_6 - t_9], [t_{12} - t_{15}], and [t_{18} - t_{21}] are the same and can be given by (1).

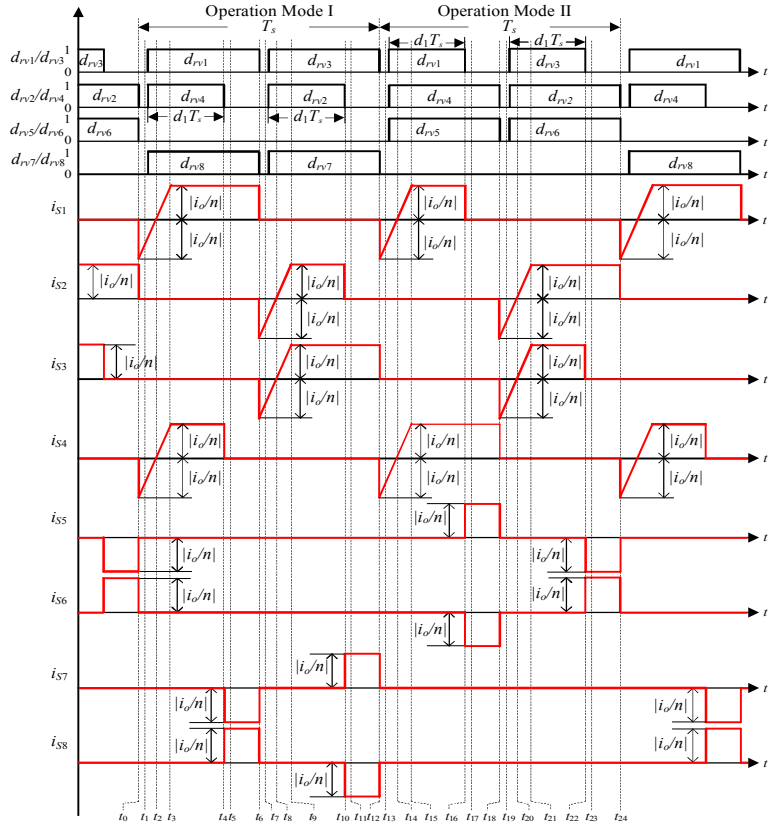


Fig. 5. Switch current waveforms under working pattern I.

$$t_3 - t_0 = t_9 - t_6 = t_{15} - t_{12} = t_{21} - t_{18} = \frac{2 \cdot L_r \cdot i_o}{n \cdot V_{in}} \quad (1)$$

Based on (1), the duty cycle loss in the one switching period T_s in the working pattern I namely d_{loss_I} can be calculated by (2).

$$d_{loss\_I} = \frac{t_3 - t_0}{T_s} = \frac{t_9 - t_6}{T_s} = \frac{t_{15} - t_{12}}{T_s} = \frac{t_{21} - t_{18}}{T_s} = \frac{2 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s} \quad (2)$$

From Fig. 5, it can be observed that: 1) the root mean square (RMS) currents of S_1, S_2, S_3, and S_4 would be the same, which are named as $i_{S1\_rms\_I}$, $i_{S2\_rms\_I}$, $i_{S3\_rms\_I}$, and $i_{S4\_rms\_I}$; 2) the RMS currents of S_5, S_6, S_7, and S_8 would be the same, which are named as $i_{S5\_rms\_I}$, $i_{S6\_rms\_I}$, $i_{S7\_rms\_I}$, and $i_{S8\_rms\_I}$; 3) the average currents of D_5, D_6, D_7, and D_8 would be the same, which are named as $i_{D5\_avg\_I}$, $i_{D6\_avg\_I}$, $i_{D7\_avg\_I}$, and $i_{D8\_avg\_I}$. According to Fig. 5 and equation (2), the RMS currents $i_{S1\_rms\_I}$ - $i_{S4\_rms\_I}$ and $i_{S5\_rms\_I}$ - $i_{S8\_rms\_I}$ and average currents $i_{D5\_avg\_I}$ - $i_{D8\_avg\_I}$ can be calculated by (3), (4), and (5) If neglecting the effect of the power switches' parasitic capacitors and dead time.

In the conventional diode clamped FB TL isolated DC/DC converter shown in Fig. 1(a), there are also two working patterns named three-level mode and two-level mode in [25]. Similar to the above analysis, the RMS currents of the primary power switches and average currents of the clamping diodes under the three-level mode can be calculated by (6), (7), and (8) if neglecting the effect of small fixed phase-shift delay between the leading and lagging power switches and dead time.

Tables II and III list the theoretical calculation equations about the RMS currents on the primary power switches, average currents on the diodes in the conventional diode clamped FB TL isolated DC/DC converter and proposed FB T-type isolated DC/DC converter. Based on Tables II and III, it can be observed that: 1) under the three-level mode in the conventional diode clamped FB TL isolated DC/DC converter, the RMS currents $i_{S1\_rms\_TL\_Con}$ and $i_{S4\_rms\_TL\_Con}$ are different from the RMS currents $i_{S2\_rms\_TL\_Con}$, $i_{S3\_rms\_TL\_Con}$, $i_{S5\_rms\_TL\_Con}$, $i_{S6\_rms\_TL\_Con}$, $i_{S7\_rms\_TL\_Con}$, and $i_{S8\_rms\_TL\_Con}$, which means that the currents among the primary power switches are unbalanced; 2) under the three-level mode in the conventional diode clamped FB TL isolated DC/DC converter, the average currents $i_{D9\_avg\_TL\_Con}$ and $i_{D10\_avg\_TL\_Con}$ are different from the average current $i_{D11\_avg\_TL\_Con}$ and $i_{D12\_avg\_TL\_Con}$, which means that the currents among the primary clamped diodes are also unbalanced; contrarily, 3) in the proposed FB T-type isolated DC/DC converter, the RMS currents among the main power switches and auxiliary power switches are the same respectively, which means that the proposed control can make the currents among the primary power switches and auxiliary power switches balanced respectively in the working pattern I.

According to Tables II, III, and circuit parameters in Appendix, the comparison results about the RMS currents of the main primary switches are presented in Fig. 6 when the input voltage V_{in} is 300 V and the output voltage V_o is 50 V. From Fig. 6, it can be observed that: 1) under the three-level mode in the conventional diode clamped FB TL isolated DC/DC converter, the RMS currents $i_{S1\_rms\_TL\_Con}$ and $i_{S4\_rms\_TL\_Con}$ are smaller than the RMS currents $i_{S2\_rms\_TL\_Con}$, $i_{S3\_rms\_TL\_Con}$, $i_{S5\_rms\_TL\_Con}$, $i_{S6\_rms\_TL\_Con}$, $i_{S7\_rms\_TL\_Con}$, and $i_{S8\_rms\_TL\_Con}$; but 2) in the proposed FB T-type isolated DC/DC converter, the RMS currents among the main power switches $i_{S1\_rms\_I}$ - $i_{S4\_rms\_I}$ are the same. Because the RMS currents on the power switches are closely related to the power losses of power switches, the current imbalance among the power switches would result in the power loss imbalance among the power switches, which would thus result in the thermal stress imbalance among the power switches. Therefore, the working pattern I can make the power loss and thermal stress among the power switches balanced in the proposed FB T-type isolated DC/DC converter, which can thus improve the reliability of the converter.

$$i_{S1\_rms\_I} = i_{S2\_rms\_I} = i_{S3\_rms\_I} = i_{S4\_rms\_I} = \sqrt{\frac{1}{2 \cdot T_s} \cdot \left[2 \cdot \int_0^{d_{loss\_I} \cdot T_S} \left(\frac{V_{in}}{L_r} \cdot t - \frac{i_o}{n} \right)^2 dt + \int_0^{(0.5 + d_1 - 2 d_{loss\_I}) \cdot T_S} \left(\frac{i_o}{n} \right)^2 dt \right]} = \sqrt{\frac{(1 + 2 \cdot d_1) \cdot i_o^2}{4 \cdot n^2} - \frac{4 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (3)$$

$$i_{S5\_rms\_I} = i_{S6\_rms\_I} = i_{S7\_rms\_I} = i_{S8\_rms\_I} = \sqrt{\frac{1}{2 \cdot T_s} \cdot \left[\int_0^{(0.5 - d_1) \cdot T_S} \left(\frac{i_o}{n} \right)^2 dt \right]} = \sqrt{\frac{(1 - 2 \cdot d_1)}{4}} \cdot \frac{i_o}{n} \quad (4)$$

$$i_{D5\_avg\_I} = i_{D6\_avg\_I} = i_{D7\_avg\_I} = i_{D8\_avg\_I} = \frac{1}{2 \cdot T_s} \cdot \int_0^{(0.5 - d_1) \cdot T_S} \frac{i_o}{n} dt = \frac{(1 - 2 \cdot d_1) \cdot i_o}{4 \cdot n} \quad (5)$$

$$i_{S1\_rms\_TL\_Con} = i_{S4\_rms\_TL\_Con} = \sqrt{\frac{V_o \cdot i_o^2}{n \cdot V_{in}} - \frac{i_o^2}{2 \cdot n^2} + \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (6)$$

$$i_{S2\_rms\_TL\_Con} = i_{S3\_rms\_TL\_Con} = i_{S5\_rms\_TL\_Con} = i_{S6\_rms\_TL\_Con} = i_{S7\_rms\_TL\_Con} = i_{S8\_rms\_TL\_Con} = \sqrt{\frac{i_o^2}{2 \cdot n^2} - \frac{4 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (7)$$

$$i_{D9\_avg\_TL\_Con} = i_{D10\_avg\_TL\_Con} = \frac{i_o}{n} - \frac{V_o \cdot i_o}{V_{in}} - \frac{4 \cdot L_r \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} \quad (8)$$

$$i_{D11\_avg\_TL\_Con} = i_{D12\_avg\_TL\_Con} = 0 \quad (9)$$

in which $i_{S1\_rms\_TL\_Con}$ - $i_{S8\_rms\_TL\_Con}$ are the RMS currents of S_1 - S_8; and $i_{D9\_avg\_TL\_Con}$ - $i_{D12\_avg\_TL\_Con}$ are the average currents of the clamping diodes D_9 - D_{12}.

TABLE II
CURRENTS ON THE PRIMARY POWER SWITCHES IN THE PROPOSED FB T-TYPE ISOLATED DC/DC CONVERTER

FB T-type isolated DC/DC converter	Working pattern I
RMS currents of S_1, S_2, S_3 and S_4	$\sqrt{\frac{(1+2\cdot d_1)\cdot i_o^2}{4\cdot n^2}-\frac{4\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}}$
RMS currents of S_5, S_6, S_7, and S_8	$\sqrt{\frac{(1-2\cdot d_1)}{4}}\cdot\frac{i_o}{n}$
Average currents of D_5, D_6, D_7, and D_8	$\frac{(1-2\cdot d_1)\cdot i_o}{4\cdot n}$

TABLE III
CURRENTS ON POWER SWITCHES AND CLAMPED DIODES IN THE CONVENTIONAL DIODE CLAMPED FB TL DC/DC CONVERTER

Conventional diode clamped FB TL DC/DC converter	Three-level mode
RMS currents of S_1 and S_4	$\sqrt{\frac{V_o\cdot i_o^2}{n\cdot V_{in}}-\frac{i_o^2}{2\cdot n^2}+\frac{8\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}}$
RMS currents of S_2, S_3, S_5, S_6, S_7, and S_8	$\sqrt{\frac{i_o^2}{2\cdot n^2}-\frac{4\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}}$
Average currents of D_9 and D_{10}	$\frac{i_o}{n}-\frac{V_o\cdot i_o}{V_{in}}-\frac{4\cdot L_r\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}$
Average currents of D_{11} and D_{12}	0

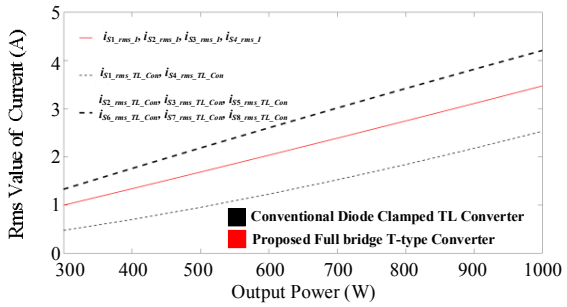


Fig. 6. Comparison results about RMS currents on main power swithes with the output power increasing (V_{in}= 300 V and V_o = 50 V).

IV. Characteristic and Performance Analysis

A. Voltage Stresses of Power Switches

In the proposed FB T-type converter with the corresponding control strategy, the main power switches S_1 - S_4 need to withstand the input voltage (V_{in}) in the steady operations, but the auxiliary power switches S_5 - S_8 only need to withstand half of the input voltage (V_{in}/2) in the steady operations.

B. Duty Cycle Loss

The duty cycle loss in the working pattern I has already analyzed in Section III, which is not repeated here.

In the working pattern II, [t_2 - t_5] and [t_8 - t_{11}] are the time periods of the duty cycle loss in the one switching period T_s as shown in Fig. 2(b). If neglecting the quite short time periods [t_2 - t_3] and [t_8 - t_9], the two time periods [t_2 - t_5] and [t_8 - t_{11}] are the same and can be given by (10).

$$t_5-t_2=t_{11}-t_8=\frac{4\cdot L_r\cdot i_o}{n\cdot V_{in}} \tag{10}$$

Based on (10), the duty cycle loss in the one switching period T_s in the working pattern II namely d_{loss_II} can be calculated by (11).

$$d_{loss\_II}=\frac{t_5-t_2}{T_s}=\frac{t_{11}-t_8}{T_s}=\frac{4\cdot L_r\cdot i_o}{n\cdot V_{in}\cdot T_s} \tag{11}$$

C. Output Characteristic

In the practical operations, the duty cycle loss would affect the output voltage. Therefore, according to the secondary voltage V_o' in Fig. 2(a) and neglecting the effect of dead time, the average output voltage in the working pattern I namely V_{o_I} can be calculated by (12) after considering the duty cycle loss (2).

$$\begin{aligned}V_{o\_I}&=\frac{2\cdot[\int_0^{(d_1-d_{loss\_I})\cdot T_s}\frac{V_{in}}{n}+\int_0^{(0.5-d_1)\cdot T_s}\frac{V_{in}}{2\cdot n}]}{T_s}\\&=\frac{V_{in}}{n}\cdot(0.5+d_1-2\cdot d_{loss\_I})=\frac{V_{in}}{n}\cdot(0.5+d_1-\frac{4\cdot L_r\cdot i_o}{n\cdot V_{in}\cdot T_s})\end{aligned} \tag{12}$$

According to the secondary voltage V_o' in Fig. 2(b) and neglecting the effect of dead time, the average output voltage in the working pattern II namely V_{o_II} can be obtained by (13) after considering the duty cycle loss (11).

$$V_{o\_II}=\frac{2\cdot[\int_0^{(d_2-d_{loss\_II})\cdot T_s}\frac{V_{in}}{2\cdot n}]}{T_s}=\frac{V_{in}}{n}\cdot(d_2-d_{loss\_II})=\frac{V_{in}}{n}\cdot(d_2-\frac{4\cdot L_r\cdot i_o}{n\cdot V_{in}\cdot T_s}) \tag{13}$$

Similar to the above analysis, the average output voltage $V_{o\_two\_level}$ in the basic FB two-level isolated DC/DC converter with the phase-shift control [32] can be obtained by (14).

$$V_{o\_two\_level}=\frac{V_{in}}{n}\cdot(2\cdot d_{two\_level}-\frac{4\cdot L_r\cdot i_o}{n\cdot V_{in}\cdot T_s}) \tag{14}$$

in which d_{two_level} is the overlap time between the leading and lagging power switch divided by one switching period as shown in Appendix (Fig. 26).

According to (12) - (14) and circuit parameters in Appendix (assuming that the FB two-level isolated DC/DC converter and proposed converter have the same transformer, secondary circuit, and switching frequency namely f_s), the theoretical relations between the input voltage V_{in} and duty cycle in the FB two-level isolated DC/DC converter and proposed converter are presented in Fig. 7 when the output power namely P_o is 1 kW and output voltage V_o is 50 V.

From Fig. 7, it can be observed that: 1) the input voltage in two converters would be the same when d_1 is 0 and d_{two_level} is 0.25; 2) the input voltage range in the working pattern I of the proposed converter is 205.9 V when the range of d_1 is [0.45 - 0], which is little wider than that in the FB two-level isolated DC/DC converter (193.2 V) when the range of d_{two_level} is [0.45 - 0.25]; 3) the input voltage range in the working pattern II of the proposed converter is 652.4 V when the range of d_2 is [0.5 - 0.2], which is much wider than that in the FB two-level isolated DC/DC converter (108.6 V) when the range of

d_{two_level} is [0.25 - 0.2]; consequently, the total input voltage range in the proposed converter is 858.3 V (205.9+652.4) when the duty cycle is from d_1 = 0.45 to d_2 =0.2, which is 2.85 times of that in the FB two-level isolated DC/DC converter with the phase-shift control (193.2+108.6 = 301.8 V) when duty cycle d_{two_level} is form 0.45 to 0.2.

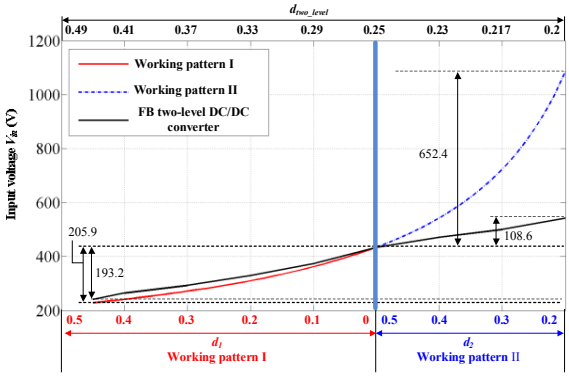


Fig. 7. Theoretical relation curves between input voltage and duty cycle when P_o = 1 kW, V_o = 50 V, and f_s = 50 KHz.

Note: In Fig. 7, the bottom X axis is usded for the working pattern I and II of the proposed converter; and the top X axis is used for the FB two-level isolated DC/DC converter with the phase-shift control [32].

D. ZVS Achievement Conditions

1) Working Pattern I

In the operation mode I, the zero-voltage switch-on of the auxiliary power switch S_7 are mainly determined by the reflected current from the output filter inductor. Normally, the output filter inductance is quiet large enough to make the auxiliary power switches achieve zero-voltage switch-on even at the light load. For instance, in order to ensure the zero-voltage switch-on of the auxiliary power switch S_7 as shown in Fig. 5, the energy E_1 is needed to discharge the capacitor C_{s2} from V_{in} to $V_{in}/2$, discharge the capacitor C_{s7} from $V_{in}/2$ to 0 V, and charge the capacitor C_{s4} from 0 V to $V_{in}/2$, whose expression can be given by (15).

In the operation mode I, the energy stored in the leakage inductor L_r (and resonant inductor if adding in the circuit) is used to realize the zero-voltage switch-on for the main power switches S_1, S_2, S_3, S_4, and auxiliary power switch S_8. For instance, in order to achieve the zero-voltage switch-on for the power switches S_1, S_4, and S_5 as shown in Fig. 5, the capacitor C_{s1} needs to be discharged from V_{in} to 0 V; the capacitors C_{s4} and C_{s5} need to be discharged from $V_{in}/2$ to 0 V; the capacitor C_{s2} needs to be charged from $V_{in}/2$ V to V_{in}; the capacitor C_{s3} needs to be charged from 0 V to V_{in}; the capacitors C_{s6} and C_{s7} need to be charged from 0 V to $V_{in}/2$. Accordingly, the following equation (16) should be satisfied to achieve the zero-voltage switch-on.

In the operation mode II, the reflected current from the output filter inductor is used to realize the zero-voltage switch-on for auxiliary power switch S_6; and the energy stored in the leakage inductor L_r (and resonant inductor if adding in the circuit) is used to realize the zero-voltage switch-on for the main power switch S_1, S_2, S_3, S_4, and auxiliary power switch S_5. However, the requirements for the power switches to achieve zero-voltage switch-on in the operation mode II are same as that in the operation mode I, which is not repeated here.

Therefore, according to (16), the load range of the ZVS achievement in the working pattern I namely $i_{o\_ZVS\_I}$ can be obtained as (17).

$$i_{o\_ZVS\_I} \ge n \cdot \sqrt{\frac{3 \cdot C_{j1} \cdot V_{in}^2}{L_r} + \frac{3 \cdot C_{j2} \cdot V_{in}^2}{4 \cdot L_r}} \tag{17}$$

2) Working Pattern II

The zero-voltage switch-on of the auxiliary power switches S_5 and S_6 are mainly determined by the reflected current from the output filter inductor. Normally, the output filter inductance is quiet large enough to make the auxiliary power switches achieve zero-voltage switch-on even at the light load. For instance, in order to ensure the zero-voltage switch-on of the auxiliary power switch S_6 as shown in Fig. 2(b), the energy E_2 is needed to discharge the capacitor C_{s3} from V_{in} to $V_{in}/2$, discharge the capacitor C_{s6} from $V_{in}/2$ to 0 V, and charge the capacitor C_{s1} from 0 V to $V_{in}/2$, whose expression can be given by (18).

The energy stored in the leakage inductor L_r (and resonant inductor if adding in the circuit) is used to realize the zero-voltage switch-on for the main power switches S_1 and S_3. For instance, in order to achieve the ZVS for the power switch S_3 as shown in Fig. 2(b), the capacitor C_{s3} needs to be fully discharged, the capacitor C_{s1} needs to be charged from $V_{in}/2$ to V_{in}, the capacitor C_{s5} needs to be charged from 0 V to $V_{in}/2$. Accordingly, the following equation (19) should be satisfied to achieve the zero-voltage switch-on of the power switch S_3.

According to (19), the load range of the ZVS achievement in the working pattern II namely $i_{o\_ZVS\_II}$ can be obtained as (20).

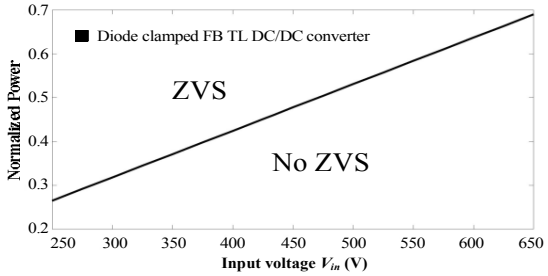
$$i_{o\_ZVS\_II} \ge n \cdot \sqrt{\frac{C_{j1} \cdot V_{in}^2}{L_r} + \frac{C_{j2} \cdot V_{in}^2}{4 \cdot L_r}} \tag{20}$$

$$E_1 \ge \frac{1}{2} \cdot C_{s2} \cdot \left[V_{in}^2 - \left(\frac{V_{in}}{2}\right)^2 \right] + \frac{1}{2} \cdot C_{s4} \cdot \left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2} \cdot C_{s7} \cdot \left(\frac{V_{in}}{2}\right)^2 = \frac{1}{2} \cdot C_{j1} \cdot V_{in}^2 + \frac{1}{8} \cdot C_{j2} \cdot V_{in}^2 \tag{15}$$

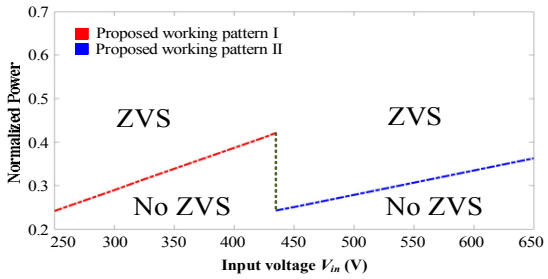
$$\begin{aligned} \frac{1}{2} L_r \cdot \left(\frac{i_o}{n}\right)^2 \ge{}& \frac{1}{2} \cdot C_{s1} \cdot V_{in}^2 + \frac{1}{2} \cdot C_{s2} \cdot \left[V_{in}^2 - \left(\frac{V_{in}}{2}\right)^2 \right] + \frac{1}{2} \cdot C_{s3} \cdot V_{in}^2 + \frac{1}{2} \cdot C_{s4} \cdot \left(\frac{V_{in}}{2}\right)^2 \\ &+ \frac{1}{2} \cdot C_{s5} \cdot \left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2} \cdot C_{s6} \cdot \left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2} \cdot C_{s7} \cdot \left(\frac{V_{in}}{2}\right)^2 = \frac{3}{2} \cdot C_{j1} \cdot V_{in}^2 + \frac{3}{8} \cdot C_{j2} \cdot V_{in}^2 \end{aligned} \tag{16}$$

Table IV presents the comparison results about the soft-switching range between the conventional diode clamped TL isolated DC/DC converter and proposed FB T-type isolated DC/DC converter. Normally, the switching loss of SiC Mosfet (C_{j_SiC}) is much smaller than that of Si Mosfet (C_{j_Si}) because the parasitic capacitor of SiC Mosfet (C_{j_SiC}) is much smaller than that of Si Mosfet (C_{j_Si}) [33]. For instance, the typical output capacitance of 900V/36A SiC Mosfet (C3M0065090D) and 650V/47A Si Mosfet (SPW47N60C3) in Table IV (in Appendix) are 60 pF and 2200 pF respectively from their datasheets. Therefore, the ZVS achievement range of the proposed convert would become larger than that of the conventional diode clamped FB TL DC/DC converter because the values of items including C_{j_Si} in the equations of the proposed converter are smaller than that of the conventional diode clamped TL DC/DC converter.

After substituting above parasitic capacitances and circuit parameters (in Appendix) into Table IV, the comparison results about theoretical ZVS load range under the conventional diode clamped FB TL DC/DC converter and proposed converter are presented in Fig. 8.



(a)



(b)

Fig. 8. Comparison results about theoretical ZVS load range. (a) Conventional diode clamped FB TL DC/DC converter. (b) Proposed FB T-type DC/DC converter. Note: Normalized power = Output power / Rated output power.

E. Output Filter Inductance

There are two kinds of working operations that $V_o \geq V_{in}/2n$ and $V_o < V_{in}/2n$ in the working pattern I.

If $V_o \geq V_{in}/2n$, the ripple current on the output filter inductor namely Δi_{Lo} is (21).

$$\Delta i_{Lo} = \frac{V_{in}/n - V_o}{L_o} \cdot (d_1 - d_{loss\_1}) \cdot T_s \tag{21}$$

If $V_o < V_{in}/2n$, the ripple current on the output filter inductor is (22).

$$\Delta i_{Lo} = \frac{V_o}{L_o} \cdot d_{loss\_1} \cdot T_s \tag{22}$$

The ripple current on the output filter inductor in the working pattern II is (23).

$$\Delta i_{Lo} = \frac{V_o}{L_o} \cdot (0.5 + d_{loss\_II} - d_2) \cdot T_s \tag{23}$$

According to (21), (22), and (23), the output filter inductance of the proposed converter with the corresponding control strategy can be obtained as (24).

$$L_o = \begin{cases} \dfrac{(\frac{V_{in}}{n} - V_o) \cdot (d_1 - d_{loss\_1}) \cdot T_s}{\Delta i_{Lo}} & \text{Operation mode I } (V_o \geq \frac{V_{in}}{2 \cdot n}) \\ \dfrac{V_o \cdot d_{loss\_1} \cdot T_s}{\Delta i_{Lo}} & \text{Operation mode I } (V_o < \frac{V_{in}}{2 \cdot n}) \\ \dfrac{V_o \cdot (1 - \frac{2 \cdot n \cdot V_o}{V_{in}}) \cdot T_s}{2 \cdot \Delta i_{Lo}} & \text{Operation mode II} \end{cases} \tag{24}$$

F. Implementation

Based on the above analysis about the working currents and voltages of the power switches in Section IV-A and Table II, the power devices can be selected after considering the derating. Normally, the rated voltage and current of chosen power devices are 1.5 times or 2 times than the steady working voltages and currents of power devices in real applications. The transformer turns ratio can be designed based on the equations (12) and (13) when giving the range of input voltage and output voltage and neglecting the effect of duty cycle loss (considering L_r at zero).

$$E_2 \geq \frac{1}{2} \cdot C_{s1} \cdot (\frac{V_{in}}{2})^2 + \frac{1}{2} \cdot C_{s3} \cdot \left[V_{in}^2 - (\frac{V_{in}}{2})^2 \right] + \frac{1}{2} \cdot C_{s6} \cdot (\frac{V_{in}}{2})^2 = \frac{1}{2} \cdot C_{j1} \cdot V_{in}^2 + \frac{1}{8} \cdot C_{j2} \cdot V_{in}^2 \tag{18}$$

$$\frac{1}{2} L_r \cdot \left(\frac{i_o}{n} \right)^2 \geq \frac{1}{2} \cdot C_{s1} \cdot \left[V_{in}^2 - (\frac{V_{in}}{2})^2 \right] + \frac{1}{2} \cdot C_{s3} \cdot (\frac{V_{in}}{2})^2 + \frac{1}{2} \cdot C_{s5} \cdot (\frac{V_{in}}{2})^2 = \frac{1}{2} \cdot C_{j1} \cdot V_{in}^2 + \frac{1}{8} \cdot C_{j2} \cdot V_{in}^2 \tag{19}$$

TABLE IV
COMPARISON RESULTS ABOUT ZVS ACHIEVEMENT RANGE

	Working pattern I (Three-level mode)	Working pattern II (Two-level mode)
Conventional diode clamped TL isolated DC/DC converter [25]	$i_o \geq n \cdot \sqrt{\frac{C_{j\_Si} \cdot V_{in}^2}{L_r}}$	
Proposed full-bridge T-type isolated DC/DC converter	$i_o \geq n \cdot \sqrt{\frac{3 \cdot C_{j\_SiC} \cdot V_{in}^2}{L_r} + \frac{3 \cdot C_{j\_Si} \cdot V_{in}^2}{4 \cdot L_r}}$	$i_o \geq n \cdot \sqrt{\frac{C_{j\_SiC} \cdot V_{in}^2}{L_r} + \frac{C_{j\_Si} \cdot V_{in}^2}{4 \cdot L_r}}$

Note: C_{j_si} and C_{j_SiC} are the parasitic capacitor of Si Mosfet and SiC Mosfet, respectively.

For the working pattern I shown in Fig. 2(a), the output voltage V_o is controlled by adjusting the duty cycle d_1 in the real application. In the first switching period, the calculated d_1 is set for the driving signals of the power switches S_2 and S_4 and duty cycle 0.5 minus the dead time is set for the driving signals of the power switches S_1 and S_3 in the first switching period; contrarily the calculated d_1 is set for the driving signals of the power switches S_1 and S_3 and duty cycle 0.5 minus the dead time is set for the driving signals of the power switches S_2 and S_4 in the second switching period. The duty cycle d_1 calculated by the control loop would be changed in every two switching periods to adjust the output voltage V_o in the steady operations. For the working pattern II shown in Fig. 2(b), the output voltage V_o is controlled by adjusting the duty cycle d_2 in the real application. (S_3, S_5) and (S_1, S_6) are complementary switch pairs; S_2 and S_4 are kept in off-state; S_7 and S_8 are kept in on-state.

Fig. 9 presents the diagram of implementation of the proposed control strategy. The proposed working pattern I and II are modulation strategy, so the conventional control algorithms (such as proportional-integral PI control) can be utilized to calculate duty cycles d_1 and d_2. As shown in Fig. 9, 1) the working pattern I is used for the low input voltage by adjusting the duty cycle d_1 from 0 to maximum value d_{1_max}; 2) when d_1 decreases to 0 due to the increasing of the input voltage, the working pattern II would be used for the higher input voltage by adjusting the duty cycle d_2.

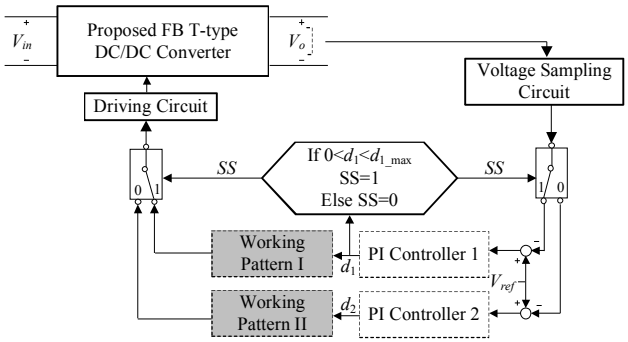


Fig. 9. Implementation of proposed control strategy.

V. Simulation And Experimental Verification

A. Simulation Verification

A simulation model is built by PLECS to verify the proposed converter with the corresponding control strategy. In the simulation model, the transformer turns ratio is 25:8; the leakage inductance of transformer is 47.7 uH; the input capacitors are output filter capacitor are 470 uF; output filter inductor is 140 uH; and the switching frequency is 50 kHz.

Fig. 10 shows the simulations results including the voltages V_{in}, V_{ab}, V_o and currents i_p, i_{Lo}, i_o when the output voltage V_o is 50 V and output power P_o is 1 kW. From Fig. 10, it can be seen that: 1) the working pattern I is utilized when the input voltage is low (300 V) as shown in Fig. 10(a); 2) the working pattern II is utilized when the input voltage is high (600 V) as shown in Fig. 10(b); and 3) the simulation results are consistent with the theoretical analysis in Section II. Fig. 11 shows the comparison results about the currents on the main primary power switches between the three-level mode of conventional diode clamped TL converter and working pattern I of proposed FB T-type converter. From Fig. 11, it can be seen that: 1) in the conventional diode clamped TL converter, the RMS values of currents i_{S1} and i_{S4} (2.584 A) are different from that of i_{S2}, i_{S3}, i_{S5}, i_{S6}, i_{S7}, and i_{S8} (4.3 A) as marked in Fig. 11(a), which means the currents among the primary power switches are unbalanced; 2) all the RMS values of currents i_{S1}, i_{S2}, i_{S3}, and i_{S4} are the same (3.6 A), which means the proposed working pattern I has the ability of balancing the currents among the primary power switches.

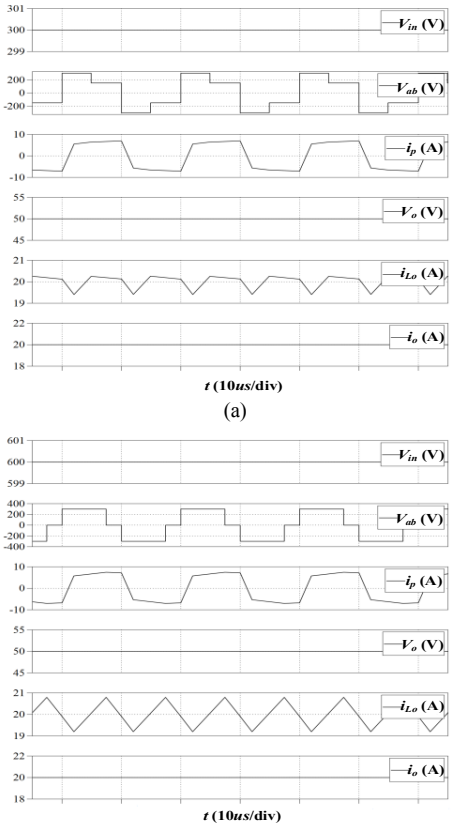
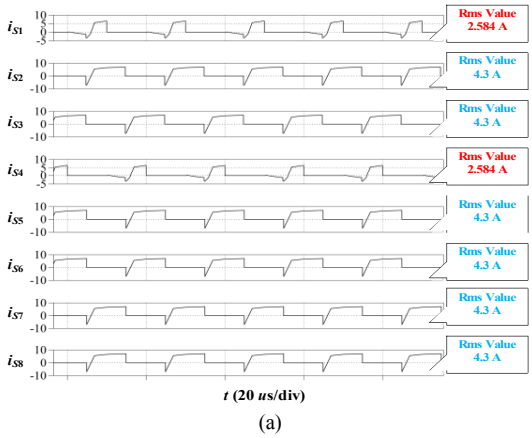
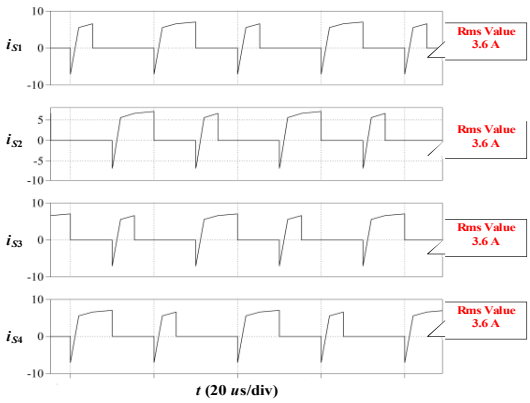


Fig. 10. Simulation results including V_{in}, V_{ab}, V_o, i_p, i_{Lo}, and i_o (V_o = 50 V and P_o = 1 kW). (a) Working pattern I (V_{in} = 300 V). (b) Working pattern II (V_{in} = 600 V).





(b)

Fig. 11. Simulation results about currents on main power switches (V_{in} = 300 V, V_o = 50 V, and P_o = 1 kW). (a) Three-level mode in conventional diode clamped TL isolated DC/DC converter. (b) Working pattern I in FB T-type isolated DC/DC converter.

B. *Experimental Verification*

In order to verify the proposed FB T-type isolated DC/DC converter with the corresponding control strategy, a 1 kW laboratory prototype is established, whose circuit parameters are listed in Appendix. Fig. 12 shows the experimental hardware of the established proposed converter.

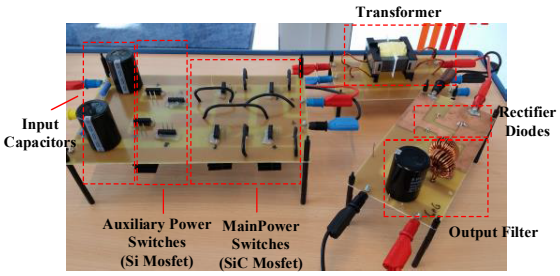


Fig. 12. Hardware of established prototype.

Figs. 13(a) and (b) show the experimental results including the voltages V_{in}, V_{ab}, V_o and current i_p under the working pattern I and II when the output voltage V_o is 50 V and output power P_o is 1 kW.

Figs. 14(a) and (b) show the voltages on the two input capacitors C_1 and C_2 (V_1 and V_2), primary voltage V_{ab}, and current on the output filter inductor i_{Lo} under the working pattern I and II when the output voltage V_o is 50 V and output power P_o is 1 kW. From Fig. 14, it can be observed that: 1) the two input voltages V_1 and V_2 are balanced and about half of the input voltage (V_{in}/2) under the working pattern I and II; and 2) the ripple current of i_{Lo} under the working pattern I is smaller than that under the working pattern II.

Figs. 15 and 16 show the drain-source voltage of the main power switches S_1 - S_4 and the auxiliary power switches S_5 - S_8 respectively under the working pattern I and II, in which V_{DS_S1} - V_{DS_S8} are the drain-source voltages of S_1 - S_8. From Figs. 15 and 16, it can be observed that: 1) the voltage stresses on the main power switches S_1 - S_4 are about the input voltage V_{in}; 2) the voltage stresses on the auxiliary power switches S_5 - S_8 are about half of the input voltage V_{in}/2; and 3) the experimental results are consistent with the theoretical analysis in Section IV-A.

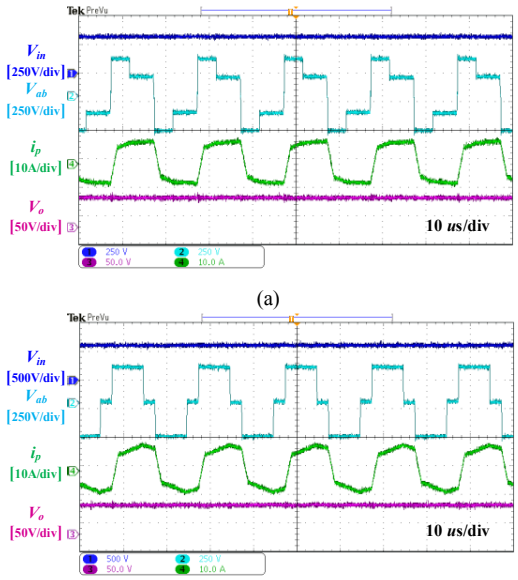


Fig. 13. Experimental results including V_{in}, V_{ab}, V_o, and i_p (V_o = 50 V and P_o = 1 kW). (a) Working pattern I (V_{in} = 300 V). (b) Working pattern II (V_{in} = 600 V).

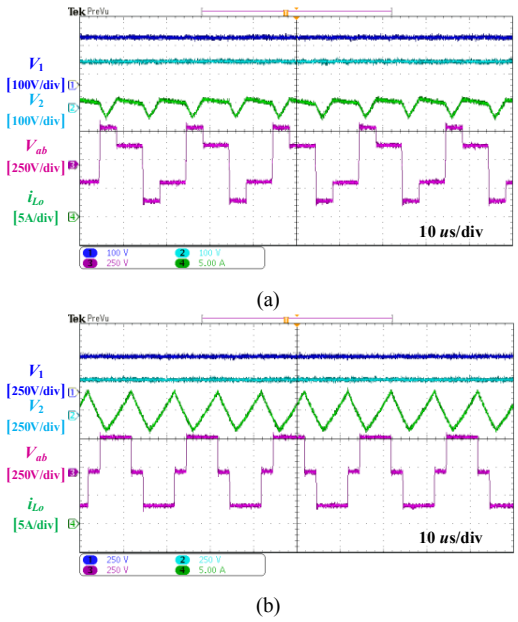


Fig. 14. Experimental results including V_1, V_2, V_{ab}, and i_{Lo} (V_o = 50 V and P_o = 1 kW). (a) Working pattern I (V_{in} = 300 V). (b) Working pattern II (V_{in} = 600 V).

Fig. 17 shows the currents flowing through the power switches under the working pattern I. Because the currents on the switch pairs (S_5, S_6) and (S_7, S_8) are similar respectively, only the currents i_{s6} and i_{s8} are shown in Fig. 17. In Fig. 17, 1) the RMS values of currents i_{S1}, i_{S2}, i_{S3}, and i_{S4} are 3.7 A, 3.72 A, 3.73 A, and 3.71 A, which are almost the same; 2) the RMS values of currents i_{s6} and i_{s8} are 3.45 A and 3.42 A, which are almost the same. Consequently, it can be concluded that the working pattern I has the ability of balancing the currents flowing through the power switches.

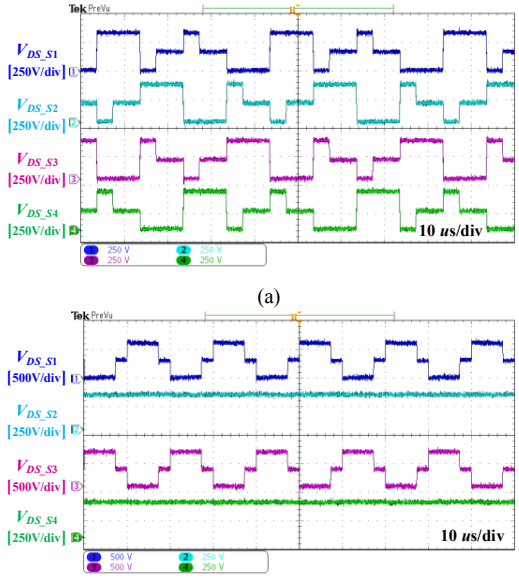


Fig. 15. Experimental results including V_{DS_S1} - V_{DS_S4} when V_o = 50 V and P_o = 1 kW. (a) Working pattern I (V_{in} = 300 V). (b) Working pattern II (V_{in} = 600 V).

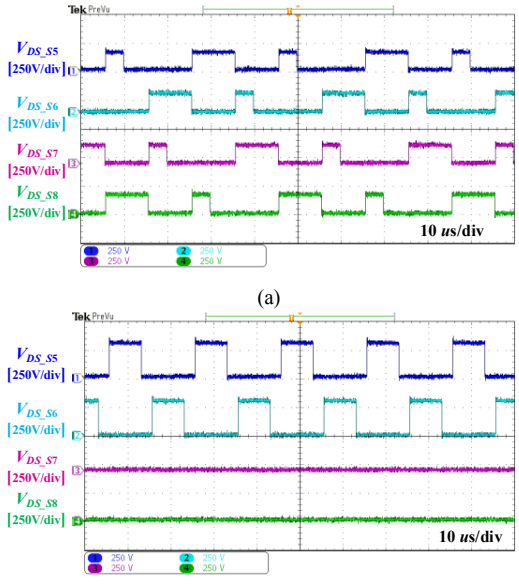
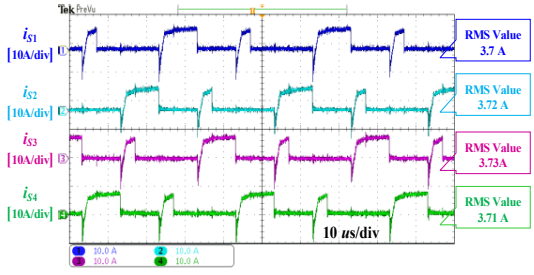


Fig. 16. Experimental results including V_{DS_S5} - V_{DS_S8} (V_o = 50 V and P_o = 1 kW). (a) Working pattern I (V_{in} = 300 V). (b) Working pattern II (V_{in} = 600 V).



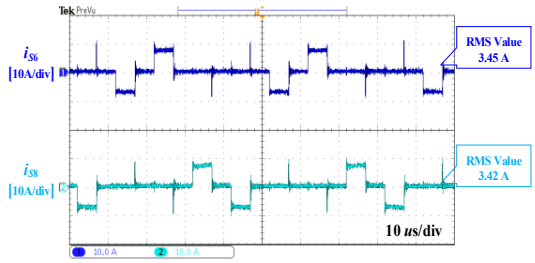


Fig. 17. Experimental results of power switch currents under working pattern I (V_o = 50 V, V_{in} = 300 V, and P_o = 1 kW). (a) i_{s1}, i_{s2}, i_{s3}, i_{s4}. (b) i_{s6}, i_{s8}.

Figs. 18(a) - (c) show the ZVS achievement performances of the main power switch S_2 under the working pattern I when the output power P_o is 1 kW, 500 W, and 125 W, in which V_{GS_S2} is the driving voltage of S_2 and i_{DS_S2} is the drain-source current of S_2. Figs. 19(a) - (c) show the ZVS achievement performances of the main power switch S_3 under the working pattern I when the output power P_o is 1 kW, 500 W, and 125 W, in which V_{GS_S3} is the driving voltage of S_3 and i_{DS_S3} is the drain-source current of S_3. Figs. 20(a) - (c) show the ZVS achievement performances of the auxiliary power switch S_6 under the working pattern I when the output power P_o is 1 kW, 500 W, and 125 W, in which V_{GS_S6} is the driving voltage of S_6 and i_{DS_S6} is the drain-source current of S_6.

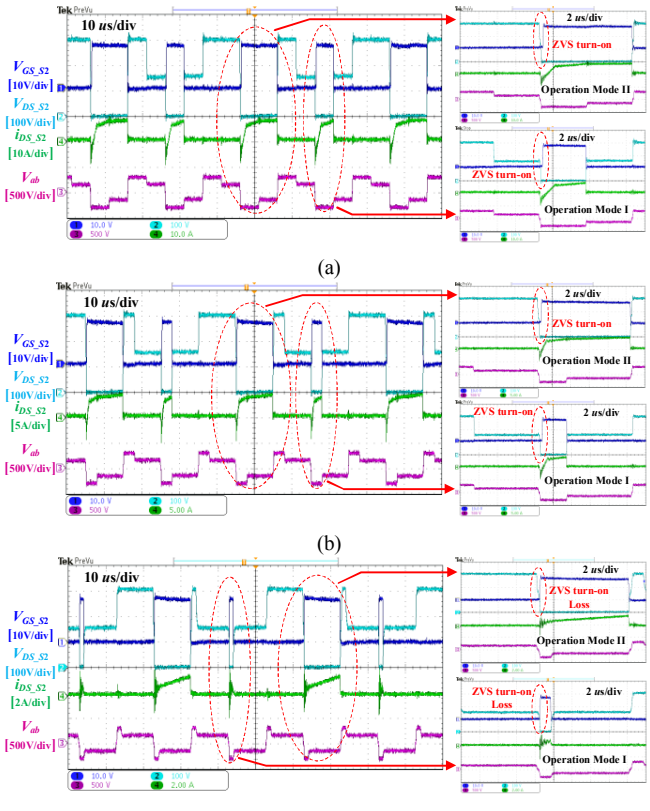


Fig. 18. ZVS achievement performances of S_2 under working pattern I (V_{in} = 300 V and V_o = 50 V). (a) P_o = 1 kW. (b) P_o = 500 W. (c) P_o = 125 W.

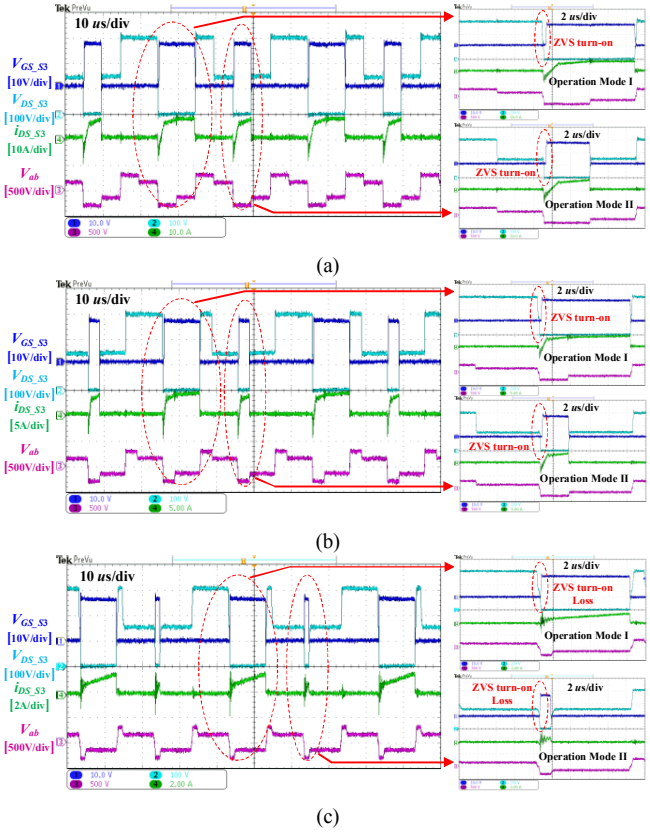


Fig. 19. ZVS achievement performances of S_3 under working pattern I (V_{in} = 300 V and V_o = 50 V). (a) P_o = 1 kW. (b) P_o = 500 W. (c) P_o = 125 W.

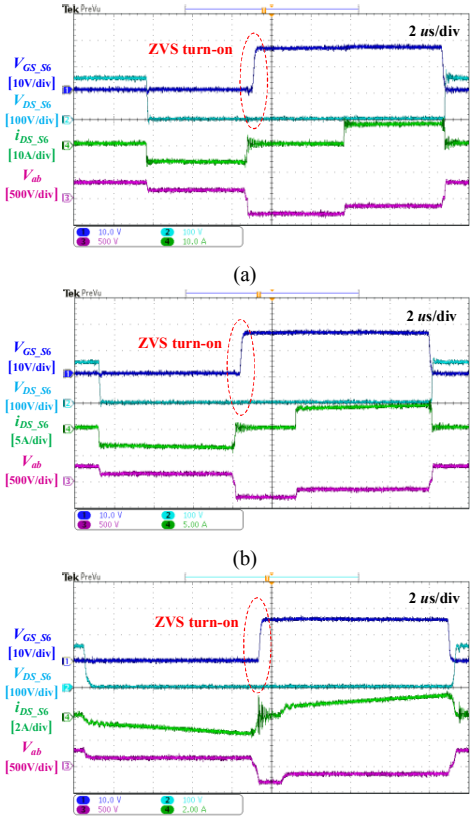


Fig. 20. ZVS achievement performances of S_6 under working pattern I (V_{in} = 300 V and V_o = 50 V). (a) P_o = 1 kW. (b) P_o = 500 W. (c) P_o = 125 W.

Figs. 21(a) - (c) show the ZVS achievement performances of the main power switch S_3 under the working pattern II when the output power P_o is 1 kW, 500 W, and 125 W. Figs. 22(a) - (c) show the ZVS achievement performances of the auxiliary power switch S_6 under the working pattern II when the output power P_o is 1 kW, 500 W, and 125 W.

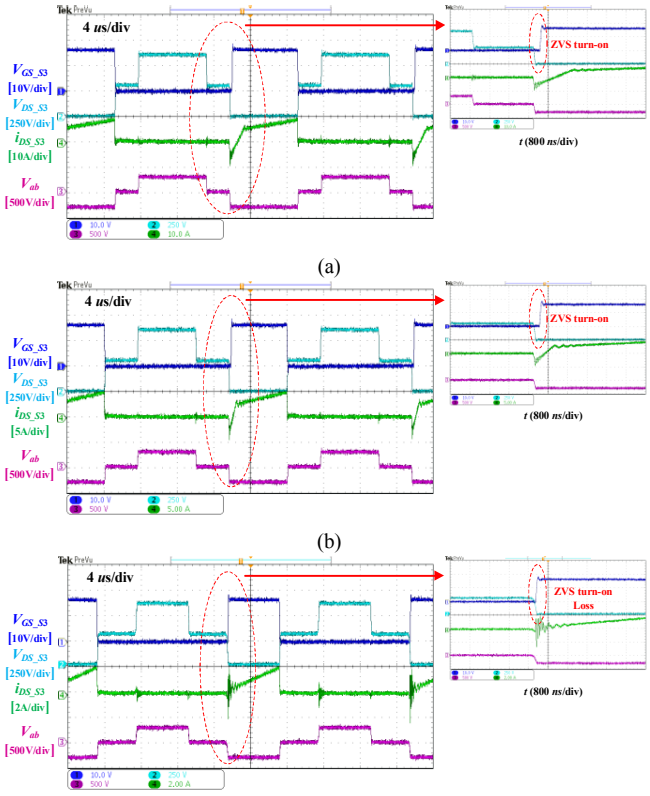
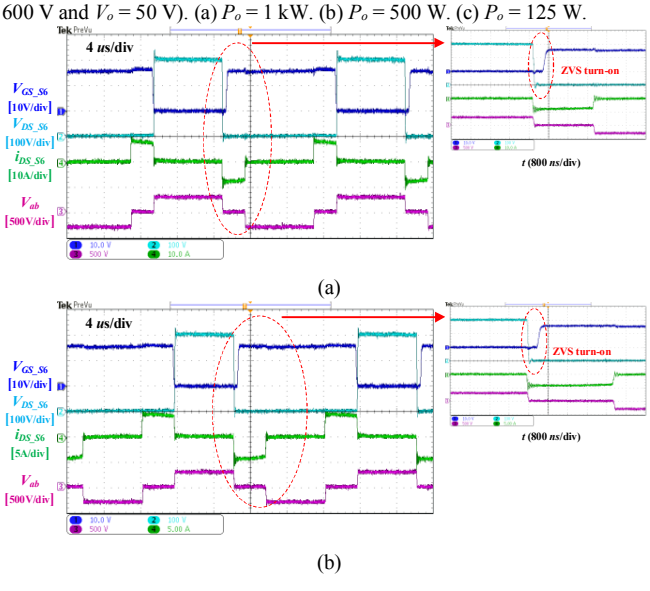
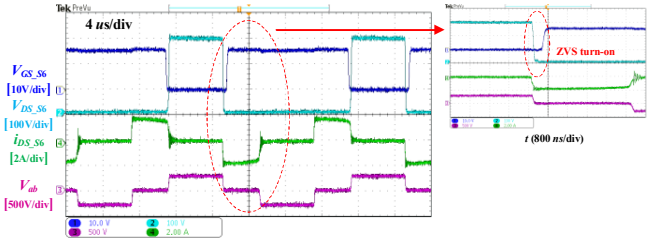


Fig. 21. ZVS achievement performances of S_3 under working pattern II (V_{in} = 600 V and V_o = 50 V). (a) P_o = 1 kW. (b) P_o = 500 W. (c) P_o = 125 W.





(c)

Fig. 22. ZVS achievement performances of S_6 under working pattern II (V_{in} = 600 V and V_o = 50 V). (a) P_o = 1 kW. (b) P_o = 500 W. (c) P_o = 125 W.

From Figs. 18 - 22, it can be observed that: 1) in the working pattern I, the main power switches S_2, S_3 and auxiliary power switch S_6 achieve the ZVS when P_o is 1 kW and 500 W respectively; the main power switches S_2, S_3 would lose the ZVS at light load (P_o is 125 W) but the auxiliary power switch S_6 can still achieve the ZVS at light load (P_o is 125 W) because the auxiliary power switch S_6 realizes the ZVS by the reflected current from the output filter inductor; and 2) in the working pattern II, the main power switch S_3 and auxiliary power switch S_6 achieve the ZVS when P_o is 1 kW and 500 W respectively; the main power switch S_3 would lose the ZVS at light load (P_o is 125 W) but the auxiliary power switch S_6 can still achieve the ZVS at light load (P_o is 125 W) because the auxiliary power switch S_6 realizes ZVS by the reflected current from the output filter inductor. The ZVS achievement performances of other main and auxiliary power switches under the working pattern I and II are similar to that of 1) and 2).

Fig. 23 shows the experimental transition performances between the proposed two working patterns under PI control, which include the input voltage (V_{in}), voltages on the two input capacitors (V_1 and V_2), and ac component of the output voltage V_o~. In Fig. 23, the input voltage steps up from 300 V to 600 V and is finally set to 260 V when the output voltage V_o is 50 V and output power P_o is 1 kW. From Fig. 23, it can be observed that there are no abnomal votlage spikes on the two input capacitors under the working pattern transitions.

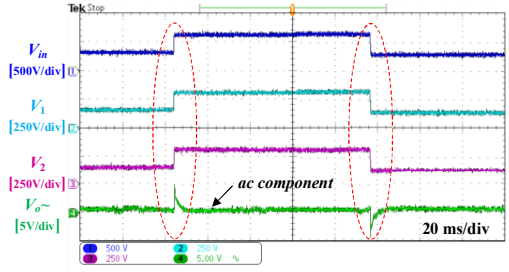


Fig. 23. Experimental transition performances between two working patterns when V_o = 50 V and P_o = 1 kW.

Fig. 24 shows the experimental efficiency curves with the various input voltages in the conventional diode clamped FB TL isolated DC/DC converter (with Si Mosfet), hybrid FB TL isolated DC/DC converter (with SiC Mosfet and Si Mosfet), and proposed FB T-type isolated DC/DC converter (with SiC Mosfet and Si Mosfet). Table V in Appendix presents the circuit components and parameters of these three established converters, in which the three converters utilize the same transformer, output rectifier, and output filter. From Fig. 24, it can be observed that the efficiencies of the proposed FB T-type isolated DC/DC converter are higher than the other two converters.

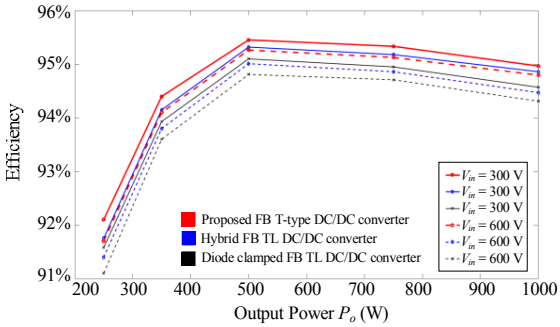
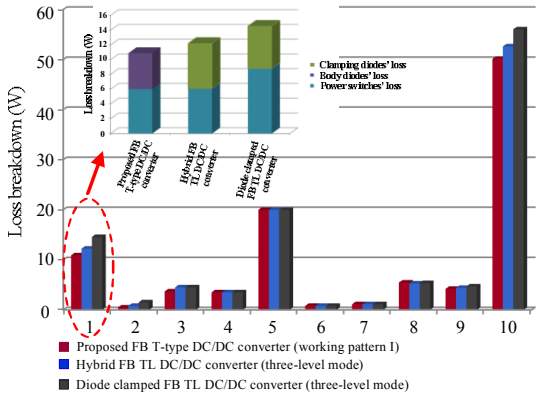
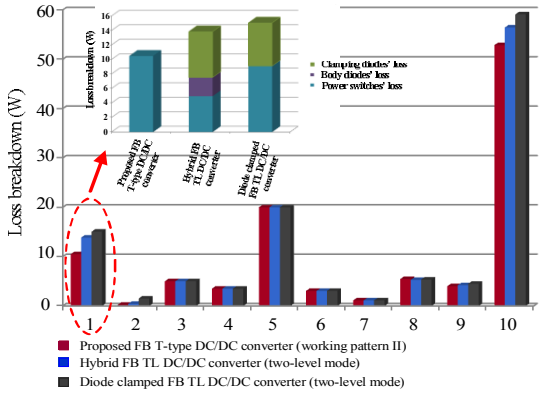


Fig. 24. Experimental comparison results about efficiencies with various input voltage when V_o = 50 V.

Fig. 25 presents the loss breakdown of main components and detailed power devices' conduction loss (including loss of power switches, loss of power switches' body diodes, and loss of clamping diodes) between the conventional diode clamped FB TL isolated DC/DC converter, hybrid FB TL isolated DC/DC converter, and proposed FB T-type isolated DC/DC converter.



(a)



(b)

Note: 1. Power devices' conduction loss; 2. Power switches' driving loss; 3. Transformer's core loss; 4. Transformer's copper loss; 5. Output rectifier diodes' loss; 6. Output filter inductor's core loss; 7. Output filter inductor's copper loss; 8. Auxiliary power supply's loss; 9. PCB loss; 10. Total loss.

Fig. 25. Comparison results about loss breakdown when V_o = 50 V, and P_o = 1 kW. (a) V_{in} = 300 V. (b) V_{in} = 600 V.

From Fig. 25, it can be observed that: 1) the conduction loss of the primary power devices in the proposed converter is smaller than that in the other two converters because the proposed convert has simpler circuit structure and there is no clamping diodes' loss in the proposed converter; 2) the driving loss of power switches in the proposed converter is smaller than that in the conventional diode clamped FB TL converter because the parasitic parameters of SiC Mosfet are much smaller than that of Si Mosfet; 3) other losses are almost the same because the three converters use the same transformer, output rectifier, output filter, and cooling fan as shown in Table V. Additionally, the power loss of output rectifier diodes occupies a large portion of the total loss in Fig. 25, the widely used methods (half-bridge output rectifier and synchronous rectification) can be further utilized to reduce it and improve the efficiency of proposed converter. However, it needs to be noticed that the synchronous rectification would cause higher cost in comparison with the diode rectification since the price of Mosfet is higher that of diode.

VI. CONCLUSION

In this paper, a FB T-type isolated DC/DC converter and a corresponding control strategy are proposed for the applications with high input voltage and wide input voltage range. The proposed FB T-type isolated DC/DC converter is composed of four main power switches with high voltage stress (SiC MOSFET) and four auxiliary power switches with low voltage stress (Si MOSFET), which thus has simpler circuit structure and higher efficiency in comparison with the conventional diode clamped FB TL isolated DC/DC converters. Additionally, a corresponding control strategy including two working patterns is also proposed, which can not only achieve the ZVS for the main and auxiliary power switches but also satisfy the wider input voltage range in comparison with the FB two-level isolated DC/DC converter. More importantly, the proposed corresponding control strategy has the switch current balancing ability, which can thus balance the power losses and thermal stress among the power switches. Finally, the simulation and experimental results both verify the effectiveness and feasibility of the proposed converter and corresponding control strategy.

APPENDIX

See Fig. 26 and Table V.

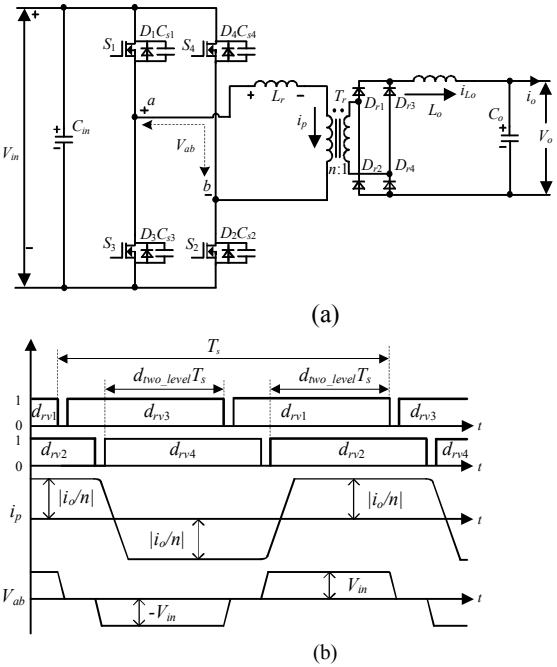


Fig. 26. (a) Basic FB two-level isolate DC/DC converter. (b) Main waveforms of basic FB two-level isolated DC/DC converter with phase-shift control.

TABLE V
CIRCUIT COMPONENTS AND PARAMETERS OF ESTABLISHED PROTOTYPE

Component		Conventional diode clamped FB TL isolated DC/DC converter	Hybrid FB TL isolated DC/DC converter	Proposed FB T-type isolated DC/DC converter
Switches	Main Power Switches	SPW47N60C3 (S_1 - S_8)	C3M0065090D (S_5, S_6)	C3M0065090D (S_1 - S_4)
	Auxiliary Power Switches		SPW47N60C3 (S_1 - S_4)	SPW47N60C3 (S_5 - S_8)
Clamping Diodes D_9 - D_{12}		DSEI30-10AR (D_9 - D_{12})	DSEI30-10AR (D_7, D_8)	/
Primary Flying Capacitor (uF)		100	100	/
Input Capacitors C_1 and C_2 (uF)		470		
Turns Ratio of the Transformer T_r		25 : 8		
Leakage Inductance L_r (uH)		47.7		
Rectifier Diodes D_{r1} - D_{r4}		MBR40250TG		
Output Filter Inductor L_o (uH)		140		
Output Filter Capacitor C_o (uF)		470		
Switching Frequency (kHz)		50		

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Dong Liu (**S**'2015 - **M**'18) received the B.Eng. and M.Sc. in electrical engineering from South China University of Technology, Guangdong, China, in 2008 and 2011, respectively. He is currently pursuing a Ph.D. in the Department of Energy Technology, Aalborg University, Denmark.

From 2011 to 2014, he was an R&D engineer in Emerson Network Power Co., Ltd., Shenzhen, China. From May, 2017 to November, 2017, he was a visiting scholar at the Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His main research interests include renewable energy technology, multilevel converters, and DC/DC converters.

Yanbo Wang (**S**'15 - **M**'17) received the M.S. degrees in electrical engineering in the Electrical Engineering School, Southwest Jiaotong University, Chengdu, China, in 2011, and received Ph.D. degree in the department of Energy Technology, Aalborg University, Denmark in 2017. Currently, he is with the department of Energy Technology in Aalborg University as a Postdoctoral Fellow.

From June to October of 2016, he was a visiting scholar in Power System Research Group of the Department of Electrical and Computer Engineering, University of Manitoba, Winnipeg, MB, Canada. His research interests include stability analysis and control of power electronic-dominated power system, distributed power generation system and active distribution network.

Fujin Deng (**S**'10 - **M**'13) received the B.Eng. degree in electrical engineering from China University of Mining and Technology, Jiangsu, China, in 2005, the M.Sc. Degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2008, and the Ph.D. degree in energy technology from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2012.

He joined the Southeast University in 2017 and is currently a Professor in the School of Electrical Engineering, Southeast University, Nanjing, China. From 2013 to 2015 and from 2015 to 2017, he was a Postdoctoral Researcher and an Assistant Professor, respectively, in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His main research interests include wind power generation, multilevel converters, high-voltage direct-current (HVDC) technology, DC grid, and offshore wind farm-power systems dynamics.

Qi Zhang (**M**'17) received the B.Eng. degree in electrical engineering from Xi'an University of Architecture and Technology, Xi'an, China, in 2004, the M.Sc. degree in Information and Control Engineering and a Ph.D. in electrical engineering from Xi'an University of Technology, Xi'an, China, in 2008 and 2012 respectively.

Since 2005, he has been with Xi'an University of Technology, where he is currently an Assistant Professor in the Department of Electrical Engineering. From 2015 to 2016, he was a Guest researcher with Aalborg University, Aalborg, Denmark. His research interests include modeling and control of power converters, bidirectional converters, and grid converters for renewable energy systems.

Zhe Chen (**M**'95 - **SM**'98) received the B.Eng. and M.Sc. degrees all in Electrical Engineering from Northeast China Institute of Electric Power Engineering, Jilin City, China, MPhil in Power Electronic, from Staffordshire University, England and the Ph.D. degree in Power and Control, from University of Durham, England.

Dr Chen is a full Professor with the Department of Energy Technology, Aalborg University, Denmark. He is the leader of Wind Power System Research program at the Department of Energy Technology, Aalborg University and the Danish Principle Investigator for Wind Energy of Sino-Danish Centre for Education and Research.

His research areas are power systems, power electronics and electric machines; and his main current research interests are wind energy and modern power systems. He has led many research projects and has more than 400 technical publications with more than 10000 citations and h-index of 44 (Google Scholar).

Dr Chen is an Associate Editor of the IEEE Transactions on Power Electronics, a Fellow of the Institution of Engineering and Technology (London, U.K.), and a Chartered Engineer in the U.K.